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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,073	03/31/2004	Alf Olsen	M4065.0752/P752	4647

7590 06/06/2006

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EXAMINER	
YAM, STEPHEN K	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 06/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,073	OLSEN ET AL.	
	Examiner	Art Unit	
	Stephen Yam	2878	

-- The MAILING DATE of this c mmunication appears n the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-32,34-82 and 84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *77-82 and 84* is/are allowed.

6)☒ Claim(s) *30-32,34-65 and 67-76* is/are rejected.

7)☒ Claim(s) *66* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to Amendments and remarks filed on March 29, 2006. Claims 30-32, 34-82, and 84 are currently pending.

Claim Objections

1. Claim 36 depends upon a cancelled claim, and thus cannot be examined.

2. Claims 68, 71, and 72 are objected to because of the following informalities:

In Claim 68, line 6, "a operational period" should be replaced with "a first operational period" for consistency.

In Claim 68, line 10, "a storage node" lacks proper antecedent basis.

In Claim 71, "the amplifier output element" lack proper antecedent basis.

In Claim 72, "the amplifier input" and "the amplifier output element" lack proper antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

> international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 30, 39, 68, 69, 72, and 75 are rejected under 35 U.S.C. 102(e) as being anticipated by Kothari et al. US Patent No. 6,552,324.

Regarding Claim 30, Kothari et al. teach (see Fig. 1-3) a pixel circuit comprising a photodetector (14) (see Fig. 1) that generates charge (see Col. 3, lines 36-38), a storage node (20) for receiving charge generated by said photodetector (see Col. 3, lines 38-40), an amplifier (33) (see Fig. 2-3) having an input coupled to said storage node (see Fig. 1 and Col. 3, lines 38-41) and an output (V_{output}) that provides an amplified input signal (see Col. 3, lines 57-59), said amplifier having a first power mode during a first operational period (see Col. 3, lines 35-37 and Col. 5, lines 10-16) and a second power mode during a second operating period (see Col. 3, lines 37-39 and Col. 5, lines 15-22), a feedback capacitor (CM1, CM2), said capacitor providing feedback between the amplifier's output and input (see Fig. 2-3), and a reset switch (within photocell) that resets said storage node when closed (since inherently, if a reset voltage is provided, the reset voltage is selectively applied to the photocell during a reset period using a switch - see Col. 1, lines 25-27).

Regarding Claim 68, Kothari et al. teach (see Fig. 1-3) an imaging circuit comprising an array of pixels (see Fig. 1 and Col. 3, lines 4-10), each pixel (15) including a photodetector (14) (see Fig. 1) that generates charge (see Col. 3, lines 36-38), a storage node (20) for receiving charge generated by said photodetector (see Col. 3, lines 38-40), an amplifier (33) (see Fig. 2-3) having an input coupled to said storage node (see Fig. 1 and Col. 3, lines 38-41), said amplifier having a first power mode during a first operational period (see Col. 3, lines 35-37 and Col. 5, lines 10-16) and a second power mode during a second operating period (see Col. 3, lines 37-39

and Col. 5, lines 15-22), a feedback capacitor (CM1, CM2) that provides feedback to an input of the amplifier (see Fig. 2-3), and a reset switch (within photocell) that resets said storage node when closed (since inherently, if a reset voltage is provided, the reset voltage is selectively applied to the photocell during a reset period using a switch - see Col. 1, lines 25-27).

Regarding Claim 75, Kothari et al. teach (see Fig. 1-3) a pixel sensor array comprising an array of pixel cells (15) (see Fig. 1 and Col. 3, lines 4-10), each pixel cell including a photodetector (14) (see Fig. 1) that generates charge (see Col. 3, lines 36-38), an amplifier (33) (see Fig. 2-3) that amplifies a signal received from said photodetector (see Col. 3, lines 38-41) said amplifier having a first power mode during an integration period (see Col. 3, lines 35-37 and Col. 5, lines 10-16) and a second power mode during a readout period (see Col. 3, lines 37-39 and Col. 5, lines 15-22), a feedback capacitor (CM1, CM2) that provides feedback to the input of the amplifier (see Fig. 2-3), and a reset switch (within photocell) that resets the photodetector from a reset voltage line when closed (since inherently, if a reset voltage is provided, the reset voltage is selectively applied to the photocell during a reset period using a switch - see Col. 1, lines 25-27).

Regarding Claim 39, Kothari et al. teach the amplifier configured as a folded four-transistor cascode amplifier (see Col. 4, lines 3-5).

Regarding Claim 69, Kothari et al. teach the amplifier as a capacitive transimpedance amplifier (since the amplifier is a folded four-transistor cascode amplifier- see Col. 3, lines 50-52 and Col. 4, lines 2-6).

Regarding Claim 72, Kothari et al. teach, for each pixel cell (15), a second select switch (50) (see Fig. 3) that connects an amplifier input to an amplifier output when closed (see Col. 5, lines 53-56).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 37, 41, 43, and 45-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kothari et al.

Regarding Claims 37, 41, and 43, Kothari et al. teach the device in Claims 30 and 39, according to the appropriate paragraph above. Regarding Claim 43, Kothari et al. teach (see Fig. 1-3) a circuit comprising a pixel array with rows and columns of pixel cells (see Col. 3, lines 7-10), and, for each row, a row readout line (22) that connects to the row's pixel cells (see Fig. 1), each pixel cell including a photodetector (14) that provides a first signal indicating detected light (see Col. 3, lines 36-38), an amplifier (33) with an input that receives the first signal and an output that provides an output signal based on the first signal (see Col. 3, lines 56-59), said amplifier having a first power mode during an integration period (see Col. 3, lines 35-37 and Col. 5, lines 10-16) and a second power mode during a readout period (see Col. 3, lines 37-39 and Col. 5, lines 15-22), and feedback capacitance (CM1, CM2) that provides feedback from the amplifier output to the amplifier input (see Fig. 2), and readout circuitry (24) connected to the

row readout line (see Fig. 1), the readout circuitry providing readout signals from the row's pixel cells (see Col. 3, lines 17-25), the readout circuitry including sampling circuitry for sampling the amplifier output signal (see Col. 3, lines 17-25). Regarding Claims 37 and 41, Kothari et al. teach a select switch (within (24)), said select switch connecting the pixel and amplifier output to a shared line (22) when closed (see Col. 3, lines 7-10 and 17-25). Kothari et al. do not teach the circuit as an integrated circuit and providing column readout as opposed to row readout (thus providing the shared line as a "column" line). It is well known in the art to construct a circuit as an integrated circuit to utilize semiconductor fabrication techniques for easier mass production, and to orient an image sensor as desired (where a row becomes a column). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the circuit as an integrated circuit and to readout in columns as opposed to rows, in the circuit of Kothari et al., to provide easier mass fabrication of the device and to provide an optimal orientation according to a desired circuitry layout.

Regarding Claim 45, Kothari et al. teach the device in Claim 43, according to the appropriate paragraph above. Kothari et al. do not teach said amplifier selectively receives a reset signal and a charge generated signal at an input, said sampling circuitry obtaining a reset sample and a charge signal sample from said amplifier output. It is well known in the art to utilize correlated double sampling (CDS) processes to read an image, whereby both a regular signal level and a reset signal level are obtained using the imaging components and the difference between the two signal levels is output as a noise-reduced signal. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide said amplifier selectively receiving a reset signal and a charge generated signal at an input, said

sampling circuitry obtaining a reset sample and a charge signal sample from said amplifier output, in the device of Kothari et al., to utilize a common CDS technique to reduce the effects of noise on the imaging capture and provide an improved output image.

Regarding Claim 46, Kothari et al. teach the amplifier as a capacitive transimpedance amplifier (since the amplifier is a folded four-transistor cascode amplifier- see Col. 3, lines 50-52 and Col. 4, lines 2-6).

Regarding Claim 47, Kothari et al. teach the amplifier including an input transistor (M1A) (see Col. 4, lines 2-6) and an output stage (see Col. 4, lines 53-56 and Col. 4, line 66 to Col. 5, line 1).

Regarding Claim 48, Kothari et al. teach the device in Claim 43, according to the appropriate paragraph above. Kothari et al. do not teach the amplifier configured as a single ended four-transistor cascode amplifier. It is well known in the art to select an appropriate amplifier type and configuration, depending on the desired operating characteristics of the circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the amplifier configured as a distributed folded four-transistor cascode amplifier, a single ended four-transistor cascode amplifier, a folded four-transistor cascode amplifier, or a differential input telescopic cascode amplifier in the circuit of Kothari et al., to provide components having the desired operating characteristics for optimal performance in the circuit.

7. Claims 31, 32, 34, 35, 42, 51, and 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kothari et al. in view of Henderson US Patent No. 6,952,004.

Regarding Claims 31, 32, and 51, Kothari et al. teach the device in Claims 30 and 43, according to the appropriate paragraph above. Kothari et al. also teach (see Fig. 1) a transfer circuit (20) that transfers charge from the photodetector to the amplifier (see Col. 3, lines 11-14, 38-41) and a switch (M9A-M9D) (see Fig. 2 and Col. 6, lines 6-20) for selectively connecting one of a first (ground) and second (full V_{bias}) power level to the amplifier, with an output power of the second power source greater than an output power of the first power source. Kothari et al. do not teach the transfer circuit as a transfer transistor or the first and second power levels from first and second power sources. Henderson teaches (see Fig. 1a, 1b) a similar device with a transfer transistor (14) that transfers said charge from a photodetector (22) to an amplifier (36) (see Fig. 1a and 1b). Further, it is well known in the art to utilize power sources to provide power levels, and to utilize a operate a device at a minimized power level as opposed to a complete shutdown, to enable quicker re-activation of the device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the transfer circuit as a transfer transistor as taught by Henderson, and to provide the first and second power levels from first and second power sources, in the device of Kothari et al., to utilize a common electronic switch component (i.e. transistor) for easier design and fabrication of the device and to enable quicker re-activation of the amplifier for faster response and minimized lag time.

Regarding Claim 34, Kothari et al. teach the device in Claim 30, according to the appropriate paragraph above. Kothari et al. do not teach the storage node as a floating diffusion node separate from the photodetector. Henderson teaches (see Fig. 1a-1b) a similar device with a storage node (Vpix) as a floating diffusion node separate from a photodetector (22) (see Fig. 1b and Col. 1, lines 22-27). It would have been obvious to one of ordinary skill in the art at the time

the invention was made to provide the storage node as a floating diffusion node separate from the photodetector, as taught by Henderson, in the device of Kothari et al., to provide improved charge accumulation characteristics for the photodetector for improved detection sensitivity.

Regarding Claim 35 and 42, Kothari et al. teach the device in Claim 30, according to the appropriate paragraph above. Kothari do not teach the reset switch resetting the feedback amplifier when closed or as a reset transistor that resets the photodetector and the feedback capacitor. Henderson teaches (see Fig. 1a, 1b) a similar device with a reset switch (16) as a reset transistor (see Fig. 1a) that resets a photodetector (22) and a feedback capacitor (Ch) when closed (see Fig. 1b and Col. 2, lines 25-29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the reset switch as a reset transistor that resets the photodetector and the feedback capacitor, as taught by Henderson, in the device of Kothari et al., to utilize a common electronic switch component (i.e. transistor) for easier design and fabrication of the device, and to discharge the components to minimize residual charges and ensure an accurate detection output.

Regarding Claim 71, Kothari et al. teach the device in Claim 68, according to the appropriate paragraph above. Kothari do not teach the array further comprises, for each pixel cell, a first select switch that connects said capacitor and said reset switch to the amplifier output circuit when closed. Henderson teaches (see Fig. 1a-1b) a similar device with a pixel array further comprises, for each pixel cell (10), a first select switch (18 in Fig. 1a, READ in Fig. 1b) that connects a feedback capacitor (Ch) and a reset switch (16) to an amplifier output when closed (see Fig. 1b). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a first select switch that connects said capacitor and said reset

switch to the amplifier output circuit when closed, as taught by Henderson, in the device of Kothari et al., to provide decoupling of the amplifier loop for improved reset properties for the amplifier.

8. Claims 38, 50, 52-57, 62-64, 67, 70, and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kothari et al. in view of Brehmer et al. US Patent No. 6,130,423.

Regarding Claims 38, 50, 52-53, 70, and 74, Kothari et al. teach the device in Claims 30, 43, and 68, according to the appropriate paragraph above. Regarding Claim 52, Kothari et al. teach the elements recited in Claim 43, according to the appropriate paragraph above. Regarding Claim 74, Kothari et al. teach the amplifier as a two-stage amplifier configured as a folded four-transistor cascode amplifier (see Fig. 2 and Col. 3, lines 50-52 and Col. 4, lines 4-6). Kothari et al. do not teach the amplifier and output stage circuitry or an output stage of the amplifier forming a distributed amplifier wherein the amplifier output stage circuitry or an output stage of the amplifier is outside the pixel array. Brehmer et al. teach (see Fig. 5 and 6) a similar integrated circuit with a pixel array (see Fig. 1) with an amplifier (621, 625) and readout circuitry (in (602)) including amplifier output stage circuitry ((505) in Fig. 5, (602) in Fig. 6) arranged such that when the pixel cell is connected to a column line the amplifier and the output stage circuitry form a distributed amplifier (see Col. 4, lines 26-27 and Col. 5, lines 23-24), with the amplifier including an input transistor (621, 625) and an output stage (505/602), with the output stage residing outside of the pixel array (see Fig. 6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the second stage of the amplifier of Kothari et al. outside the pixel array to form a distributed amplifier, as taught by

Brehmer et al., in the device of Kothari et al., to reduce the complexity and number of components of the system by sharing a portion of the amplification process among multiple pixel cells, as taught by Brehmer et al. (see Col. 3, lines 46-61).

Regarding Claim 54, Kothari et al. teach select circuitry (within (33)) that connects a pixel cell to an associated row readout line in response to a select signal (ΦPIX) (see Col. 3, lines 17-20).

Regarding Claim 56, Kothari et al. teach the two-stage amplifier configured as a folded four-transistor cascode amplifier (see Col. 3, lines 50-52 and Col. 4, lines 4-6).

Regarding Claim 62, Kothari et al. teach the photodetector sensing visible light (since the device is used as a document reader- see Col. 3, lines 27-31).

Regarding Claim 63, Kothari et al. in view of Brehmer et al. teach the device in Claim 52, according to the appropriate paragraph above. Kothari et al. do not teach the photodetector sensing infrared light. It is well known in the art to configure an imaging device to sense either visible light or infrared light, depending on the desired application for the imaging device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the photodetector sensing infrared light, in the device of Henderson, to provide appropriate detection characteristics for a specific desired imaging operation.

Regarding Claims 55 and 57, Kothari et al. in view of Brehmer et al. teach the device in Claim 43, according to the appropriate paragraph above. Kothari et al. do not teach the amplifier configured as a single ended four-transistor cascode amplifier or a differential input telescopic cascode amplifier. It is well known in the art to select an appropriate amplifier type and configuration, depending on the desired operating characteristics of the circuit. It would have

been obvious to one of ordinary skill in the art at the time the invention was made to provide the amplifier configured as a single ended four-transistor cascode amplifier or a differential input telescopic cascode amplifier in the circuit of Kothari et al. in view of Brehmer et al., to provide components having the desired operating characteristics for optimal performance in the circuit.

Regarding Claim 64, inherently, since a reset voltage is provided, the reset voltage is selectively applied to the photocell during a reset period using a switch (see Col. 1, lines 25-27).

Regarding Claim 67, Kothari et al. teach the readout circuitry further including a sampling circuit connected to each row readout line (see Col. 3, lines 17-25).

9. Claims 40, 44, 49, 58-61, 65, 73, and 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kothari et al. (in view of Brehmer et al. for Claims 54, 58 and 65) in view of Henderson.

Regarding Claims 40, 44, 49, 58, 73, and 76, Kothari et al. (in view of Brehmer et al. for Claims 58 and 78) teach the device in Claims 34, 43, 48, and 68, according to the appropriate paragraph above. Kothari et al. also teach (see Fig. 1) a transfer circuit (20) that transfers charge from the photodetector to the amplifier (see Col. 3, lines 11-14, 38-41). Kothari et al. do not teach the transfer circuit as a transfer transistor. Henderson teaches (see Fig. 1a, 1b) a similar device with a transfer transistor (14) that transfers said charge from a photodetector (22) to an amplifier (36) (see Fig. 1a and 1b). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the transfer circuit as a transfer transistor as taught by Henderson in the device of Kothari et al. (in view of Brehmer et al. for Claims 58 and 78), to

utilize a common electronic switch component (i.e. transistor) for easier design and fabrication of the device.

Regarding Claim 60, Kothari et al. teach the two-stage amplifier configured as a folded four-transistor cascode amplifier (see Col. 3, lines 50-52 and Col. 4, lines 4-6).

Regarding Claims 59 and 61, Kothari et al. in view of Brehmer et al. and Henderson teach the device in Claim 58, according to the appropriate paragraph above. Kothari et al. do not teach the amplifier configured as a single ended four-transistor cascode amplifier or a differential input telescopic cascode amplifier. It is well known in the art to select an appropriate amplifier type and configuration, depending on the desired operating characteristics of the circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the amplifier configured as a single ended four-transistor cascode amplifier or a differential input telescopic cascode amplifier in the circuit of Kothari et al. in view of Brehmer et al. and Henderson, to provide components having the desired operating characteristics for optimal performance in the circuit.

Regarding Claim 65, Kothari et al. in view of Brehmer et al. teach the device in Claim 52, according to the appropriate paragraph above. Kothari do not teach the reset switch resetting the photodetector *and the amplifier* to a reset level. Henderson teaches (see Fig. 1a, 1b) a similar device with a reset switch (16) as a reset transistor (see Fig. 1a) that resets a photodetector (22) and a feedback capacitor (Ch) for an amplifier (36) to a reset level (see Fig. 1b and Col. 2, lines 25-29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the reset switch that resets the photodetector and the amplifier to a reset level, as taught by Henderson, in the device of Kothari et al., to utilize a common electronic

switch component (i.e. transistor) for easier design and fabrication of the device, and to discharge the components to minimize residual charges and ensure an accurate detection output.

Allowable Subject Matter

10. Claims 77-82 and 84 are allowed over the prior art of record.

11. Claim 66 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claim 66, the invention as claimed, specifically in combination with each pixel further including a reset switch that, when closed, resets the amplifier and a floating diffusion node coupled to the photodetector and to the input of said amplifier, is not disclosed or made obvious by the prior art of record.

Regarding Claim 77, the invention as claimed, specifically in combination with the amplifier having a first power mode during an integration period and a second power mode during a readout period, with amplifier output circuitry located outside the pixel array; and the amplifier, the amplifier output circuitry, and the feedback capacitor together forming a capacitive transimpedance amplifier, is not disclosed or made obvious by the prior art of record.

Response to Arguments

13. Applicant's arguments with respect to claims 30-32, 34-82, and 84 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Miyamoto US Patent No. 6,875,356 teach a similar device with providing multiple power settings for an amplifier.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Yam whose telephone number is (571)272-2449. The examiner can normally be reached on Monday-Friday 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on (571)272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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THANH X. LUU
PRIMARY EXAMINER